

## DUAL BUS BUFFER

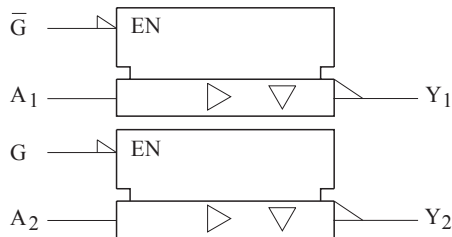
### FEATURES

- Super High Speed :  $t_{PD}=2.3ns$ (Typ.) into 50pF at  $V_{CC}=5V$ .
- High Output Driver :  $\pm 24mA$  at  $V_{CC}=3V$ .
- Power Down High Impedance inputs/outputs.
- Outputs are Overvoltage Tolerant is 3-STATE mode.
- Wide Operating Voltage Range :  $V_{CC(opr)}=1.65\sim 5.5V$ .

### MAXIMUM RATINGS (Ta=25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	$V_{CC}$	-0.5~7	V
DC Input Voltage	$V_{IN}$	-0.5~7	V
DC Output Voltage	$V_{OUT}$	-0.5~7	V
Input Diode Current	$I_{IK}$	-50	mA
Output Diode Current	$I_{OK}$	-50	mA
DC Output Current	$I_{OUT}$	$\pm 50$	mA
DC $V_{CC}$ /ground Current	$I_{CC}$	$\pm 100$	mA
Power Dissipation	$P_D$	200	mW
Storage Temperature Range	$T_{stg}$	-65 ~ 150	°C
Lead Temperature (10s)	$T_L$	260	°C

### Logic Diagram

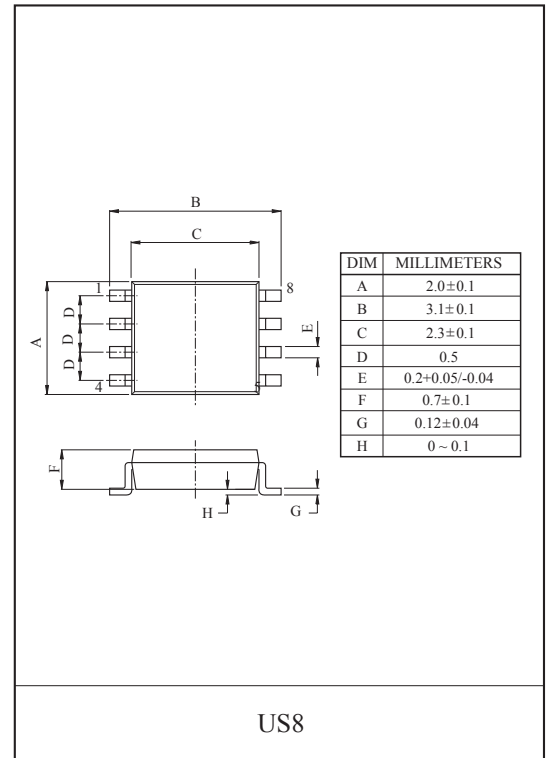


### Truth Table

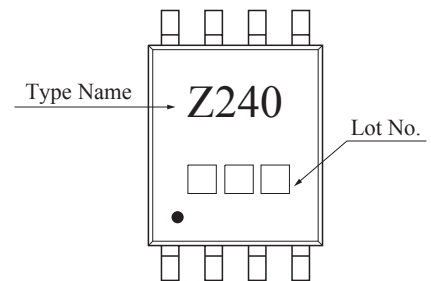
INPUTS			OUTPUTS
$\bar{G}$	G	A	Y
L	H	L	L
L	H	H	H
H	L	X	Z

X : Don't Care

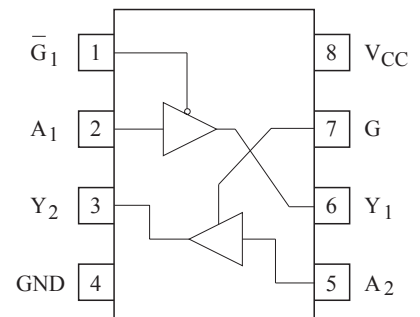
Z : High Impedance



### MARKING



### PIN CONNECTION(TOP VIEW)



# KIC7WZ240FK

## Recommended Operating Conditions

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	$V_{CC}$	1.65~5.5	V
		1.5~5.5 (Note1)	
Input Voltage	$V_{IN}$	0~ $V_{CC}$	V
Output Voltage	$V_{OUT}$	0~ $V_{CC}$ (Note2)	V
		0~5.5 (Note3)	
Operating Temperature	$T_{opr}$	-40~85	°C
Input Rise and Fall Time	$t_r, t_f$	0~20 ( $V_{CC}=1.8\pm 0.15V, 2.5\pm 0.2V$ ) 0~10 ( $V_{CC}=3.8V\pm 0.3V$ ) 0~5 ( $V_{CC}=5.0V\pm 0.5V$ )	ns/V

Note1 : Data retention only. Note2 : Active State. Note3 : 3-STATE

## ELECTRICAL CHARACTERISTICS (DC Characteristics)

CHARACTERISTIC		SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT	
				$V_{CC}(V)$	MIN.	TYP.	MAX.	MIN.	MAX.		
Input Voltage	High Level	$V_{IH}$	-	1.65~1.95	$0.75 \times V_{CC}$	-	-	$0.75 \times V_{CC}$	-	V	
				2.3~5.5	$0.7 \times V_{CC}$	-	-	$0.7 \times V_{CC}$	-		
	Low Level	$V_{IL}$		1.65~1.95	-	-	$0.25 \times V_{CC}$	-	$0.25 \times V_{CC}$		
				2.3~5.5	-	-	$0.3 \times V_{CC}$	-	$0.3 \times V_{CC}$		
Output Voltage	High Level	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$	$I_{OH}=-100\mu A$	1.65	1.55	1.65	-	1.55	-	V
					2.3	2.2	2.3	-	2.2	-	
					3.0	2.9	3.0	-	2.9	-	
					4.5	4.4	4.5	-	4.4	-	
				$I_{OH}=-4mA$	1.65	1.29	1.52	-	1.29	-	
				$I_{OH}=-8mA$	2.3	1.9	2.15	-	1.9	-	
				$I_{OH}=-16mA$	3.0	2.4	2.80	-	2.4	-	
				$I_{OH}=-24mA$	3.0	2.3	3.68	-	2.3	-	
	Low Level	$V_{OL}$		$I_{OL}=100\mu A$	1.65	-	0	0.1	-	0.1	V
					2.3	-	0	0.1	-	0.1	
					3.0	-	0	0.1	-	0.1	
					4.5	-	0	0.1	-	0.1	
				$I_{OL}=4mA$	1.65	-	0.08	0.24	-	0.24	
				$I_{OL}=8mA$	2.3	-	0.10	0.30	-	0.30	
				$I_{OL}=16mA$	3.0	-	0.15	0.40	-	0.40	
				$I_{OL}=24mA$	3.0	-	0.22	0.55	-	0.55	
Input Leakage Current		$I_{IN}$	$V_{IN}=5.5V$ or GND	0~5.5	-	-	$\pm 0.1$	-	$\pm 1$	$\mu A$	
3-STATE Output Leakage		$I_{OZ}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $0 \leq V_{OUT} \leq 5.5V$	1.65~5.5	-	-	$\pm 0.5$	-	$\pm 5$	$\mu A$	
Power Off Leakage Current		$I_{OFF}$	$V_{IN}$ or $V_{OUT}=5.5V$	0.0	-	-	1	-	10	$\mu A$	
Quiescent Supply Current		$I_{CC}$	$V_{IN}=5.5V$ or GND	1.65~5.5	-	-	1	-	10	$\mu A$	

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## Noise Characteristics

CHARACTERISTIC	SYMBOL	TEST CONDITION		Ta=-25°C		UNIT
			V <sub>CC</sub> (V)	TYP.	MAX.	
Quiet Output Maximum Dynamic V <sub>OL</sub>	V <sub>OLP</sub> (Note 1)	C <sub>L</sub> =50pF	5.0	-	1.0	V
Quiet Output Minimum Dynamic V <sub>OL</sub>	V <sub>OLV</sub> (Note 1)	C <sub>L</sub> =50pF	5.0	-	1.0	V
Quiet Output Minimum Dynamic V <sub>OH</sub>	V <sub>OHV</sub> (Note 1)	C <sub>L</sub> =50pF	5.0	-	4.0	V
Minimum HIGH Level Dynamic Input Voltage	V <sub>IHD</sub> (Note 1)	C <sub>L</sub> =50pF	5.0	-	3.5	V
Maximum LOW Level Dynamic Input Voltage	V <sub>ILD</sub> (Note 1)	C <sub>L</sub> =50pF	5.0	-	1.5	V

Note 1 : Characteristic guaranteed by design.

## AC Characteristics

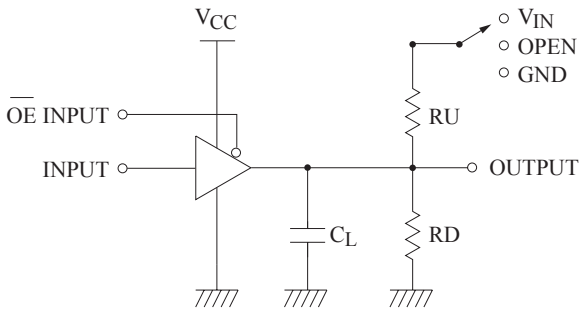
CHARACTERISTIC	SYMBOL	TEST CONDITION	Ta=25°C			Ta=-40~85°C		UNIT	
			V <sub>CC</sub> (V)	MIN.	TYP.	MAX.	MIN.		MAX.
Propagation Delay A <sub>N</sub> to Y <sub>N</sub> (Figures 1,3)	t <sub>PLH</sub> t <sub>PHL</sub>	C <sub>L</sub> =15pF, R <sub>D</sub> =1MΩ S1=Open	1.8±0.15	2.0	-	12.0	2.0	13.0	ns
			2.5±0.2	1.0	-	7.5	1.0	8.0	
			3.3±0.3	0.8	-	5.2	0.8	5.5	
			5.0±0.5	0.5	-	4.5	0.5	4.8	
	t <sub>PLH</sub> t <sub>PHL</sub>	C <sub>L</sub> =50pF, R <sub>D</sub> =500Ω S1=Open	3.3±0.3	1.2	-	5.7	1.2	6.0	ns
			5.0±0.5	0.8	-	5.0	0.8	5.3	
Output to Output Skew (Figures 1,3) (Note 2)	t <sub>OSLH</sub> t <sub>OSHL</sub>	C <sub>L</sub> =50pF, R <sub>D</sub> =500Ω S1=Open	3.3±0.3	-	-	1.0	-	1.0	ns
			5.0±0.5	-	-	0.8	-	0.8	
Output Enable Time (Figures 1,3)	t <sub>PZL</sub> t <sub>PZH</sub>	C <sub>L</sub> =50pF, R <sub>D</sub> , R <sub>U</sub> =500Ω S1=GND for t <sub>PZH</sub> S1=V <sub>1</sub> for t <sub>PZL</sub> V <sub>1</sub> =2×V <sub>CC</sub>	1.8±0.15	3.0	-	14.0	3.0	15.0	ns
			2.5±0.2	1.8	-	8.5	1.8	9.0	
			3.3±0.3	1.2	-	6.2	1.2	6.5	
			5.0±0.5	0.8	-	5.5	0.8	5.8	
Output Disable Time (Figures 1,3)	t <sub>PLZ</sub> t <sub>PHZ</sub>	C <sub>L</sub> =50pF, R <sub>D</sub> , R <sub>U</sub> =500Ω S1=GND for t <sub>PHZ</sub> S1=V <sub>1</sub> for t <sub>PLZ</sub> V <sub>1</sub> =2×V <sub>CC</sub>	1.8±0.15	2.5	-	12.0	2.5	13.0	ns
			2.5±0.2	1.5	-	8.0	1.5	8.5	
			3.3±0.3	0.8	-	5.7	0.8	6.0	
			5.0±0.5	0.3	-	4.7	0.3	5.0	
Input Capacitance	C <sub>IN</sub>		0	-	2.5	-	-	pF	
Output Capacitance	C <sub>OUT</sub>		5.0	-	4	-	-	pF	
Power Dissipation Capacitance (Figure 2)	C <sub>PD</sub>	(Note 3)	3.3	-	10	-	-	-	pF
			5.0	-	12	-	-	-	

Note 2 : Characteristic guaranteed by design. t<sub>OSLH</sub>=|t<sub>PLHmax</sub>-t<sub>PLHmin</sub>| ; t<sub>OSHL</sub>=|t<sub>PHLmax</sub>-t<sub>PHLmin</sub>|.

Note 3 : C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I<sub>CCD</sub>) at no output loading and operating at 50% duty cycle. (See Figure 2.) C<sub>PD</sub> is related to I<sub>CCD</sub> dynamic operating current by the expression : I<sub>CCD</sub>=C<sub>PD</sub> · V<sub>CC</sub> · f<sub>IN</sub>+I<sub>CC</sub>

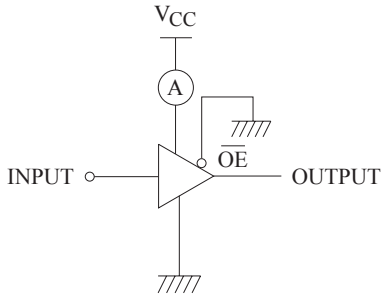
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## AC Loading and Waveforms



$C_L$  includes load and stray capacitance  
 Input PRR=1.0MHz ;  $t_w=500ns$

FIGURE 1. AC Test Circuit



Input=AC Waveform ;  $t_r=t_f=1.8ns$ ;  
 PRR=10MHz ; Duty Cycle=50%

FIGURE 2. ICCD Test Circuit

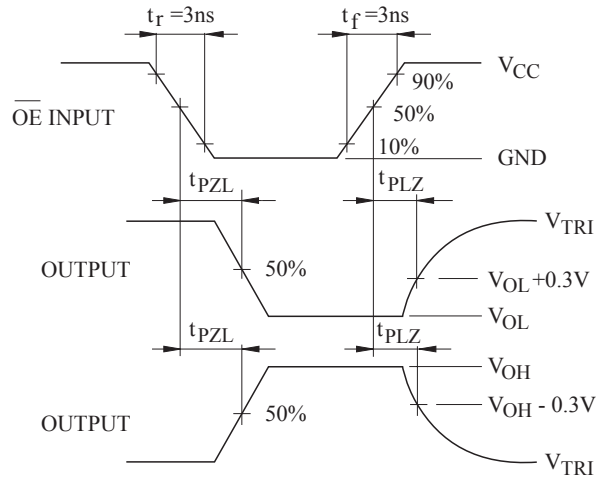
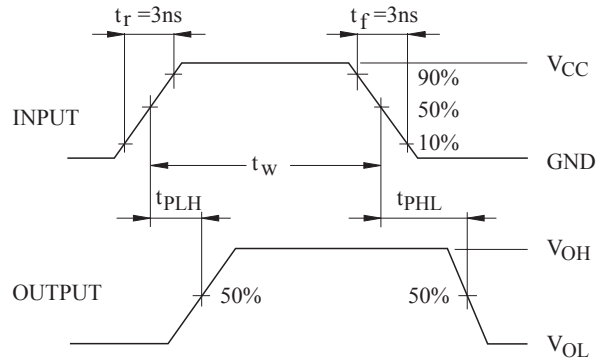


FIGURE 3. AC Waveforms